REMARKS

Claims 1-7 and 27-39 are pending in the present application.

Claim 1 was amended to conform to the claims in the parent application; claims 5-6 were amended to correct typographical errors.

Claims 27-39 were added.

Examination of the application on the merits is respectfully requested.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claims 1 and 5-6 were amended herein as follows:

1. (amended) A CMOS integrated circuit device comprising:

a plurality of p-channel transistors formed in active surface areas of n-type regions, wherein the p-channel transistors do not have LDD source/drain regions;

a plurality of n-channel transistors formed in isolated active surface areas of p-type regions;

gate electrodes for the p-channel and n-channel transistors, the gate electrodes overlying and being insulated from the respective active surface areas, wherein the gate electrodes for the p-channel transistors have a width less than a minimum channel length required for the p-channel transistors;

p-type source and drain regions for the p-channel transistors, each p-type source and drain region consisting of a low resistivity region;

n-type source and drain regions for the n-channel transistors, each n-type source and drain region having a low resistivity region and an LDD region;

each gate electrode having a pair of sidewall spacers each having an inner and an outer portion, [each sidewall spacer corresponding to an underlying source and drain region]wherein

the inner portions of the sidewall spacers for each p-channel transistor gate electrode has a width which, taken on each side of the respective gate electrode for the respective p-channel transistor and combined with the width of the respective gate electrode for the respective p-channel transistor, exceeds a minimum channel length for the respective p-channel transistor;

each p-channel low resistivity region located under the outer portion and at least a part of the inner portion of its respective sidewall spacer;

each n-channel low resistivity region located under at least a part of the outer portion and a part of the inner portion of its respective sidewall spacer; and

each n-channel LDD region extending from its respective low resistivity region to underlie the inner portion of its respective sidewall spacer.

5. (amended) The integrated circuit of claim 1, wherein:

the distance between low resistivity regions of the source and drain regions of the p-channel transistor is between the p-channel minimum length and the p-channel maximum length, wherein:

the p-channel minimum length is a distance below which the transistor will not operate reliably due to short channel effects; and

the p-channel maximum length is a distance [the] above which the transistor will not turn on efficiently.

6. (amended) The integrated circuit of claim 1, wherein:

the distance between the low resistivity regions of the n-channel transistor is between the n-channel minimum LDD length and the n-channel maximum LDD length, wherein:

the n-channel minimum LDD length is a distance below which the transistor will not operate reliably due to short channel effects; and

the n-channel maximum LDD length is a distance above which the transistor will not turn on efficiently.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@novakov.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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